

PBAR NOTE #635
INVESTIGATIONS INTO ACCUMULATOR 4-8 GHZ
PICKUP LOOP / COMBINER BOARD PERFORMANCE

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Introduction

A set of pickup measurements performed in August of 1999 (see **Pbar note 618**) indicated problems with the pickup sensitivity for frequencies above ~ 4.8 GHz. This note describes the effort made to determine if the problems with system performance were due to the design of the 4-8 GHz circuit board.

4-8 GHz loop design

The first thing looked at was the present 4-8 GHz loop design. A Tektronics TDR was used to determine the impedance match through the loop and an S_{11} measurement was done to see in-band reflections (see Figures 1 & 2). The thought was the match was poor and should be improved so the S_{11} measurement was better than -20dB across the 4-8 GHz band. Also, based on the measurements in **Pbar note 618**, the loop center frequency was too low and needed to be raised to improve response in the upper half of the band.

An improved loop was built and tested in November 1999 (see Figures 3 & 4). After completion, a set of prototype boards were made and installed in the Accumulator 4-8 GHz vertical tank. Measurements of the magnitude and sensitivity of this new smaller loop were disappointing. The smaller loop was considerably less sensitive than the old loop, and moving the center frequency up did not help the problem with the steep gain slope above 4.8 GHz (see Figure 5). It was determined from these results that the problems lay elsewhere, perhaps in the combiner section.

4-8 GHz Combiner section

The combiner section was put through two tests. The first looked at magnitude and phase characteristics of individual combiner paths, and the second was a vector summation with measured data from each of the 32 possible paths through the combiner.

An actual 4-8 GHz board was modified for these tests. Using a razor and straight edge, each of the 32 loops on the board was trimmed to a 100 Ω transmission line and the holes in the ground plane covered with copper tape. The board was then mounted in an actual kicker backplane with all the normal hardware and ferrites.

Test number one revealed no problems (see Figures 6 \rightarrow 8). S_{21} measurements were made through both the longest and shortest combiner paths. There is only about a 2dB gain slope through any given combiner path, so the contribution from microstrip losses on the board to the gain slope seen in the pickup response is small. Also, the difference in attenuation between the longest and shortest paths is only 2dB at the upper end of the band and is again of no consequence.

Test two was more ambitious and was intended to identify any problems with the actual combining of the signals. An S_{21} measurement was done for each of the 32-combiner legs and the electrical delay calculated using LABVIEW. This data was put into an EXCEL spreadsheet where a vector summation was done. Again, the results did not indicate any problems like those seen in the original measurements (see Figure 9).

Conclusions

Based on the tests done, it seems clear the current 4-8 GHz board design is not the source of the gain slope. The best guess at this point is a problem with modes propagating down the beamline. Studies to investigate this possibility are in the works and will be the subject of a future Pbar note.

Figure 1: Impedance match through current 4-8 GHz loop.

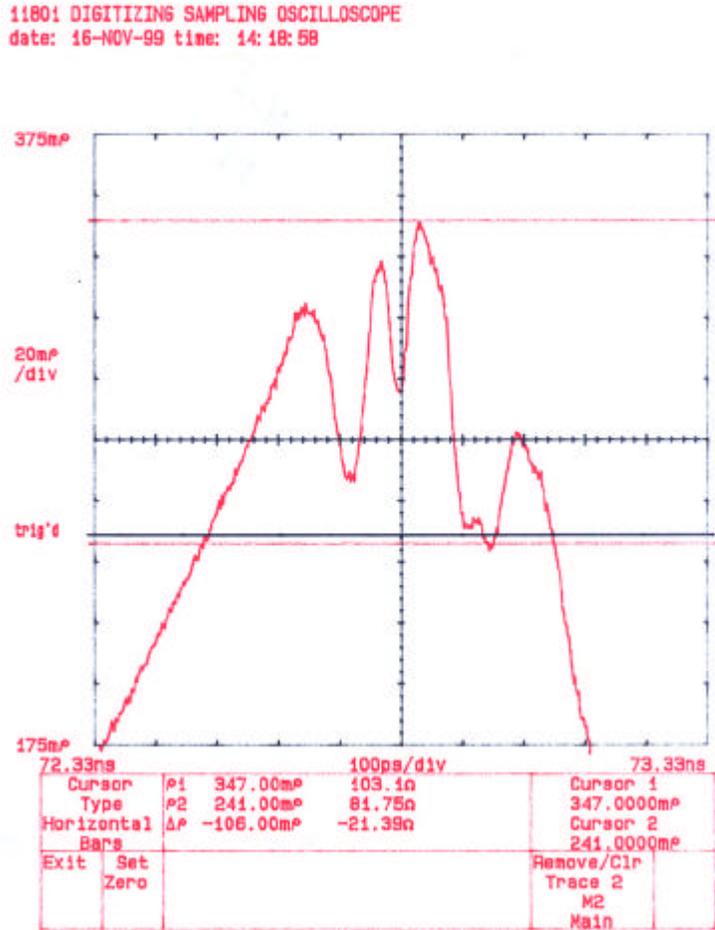


Figure 2: S_{11} of current 4-8 GHz loop.

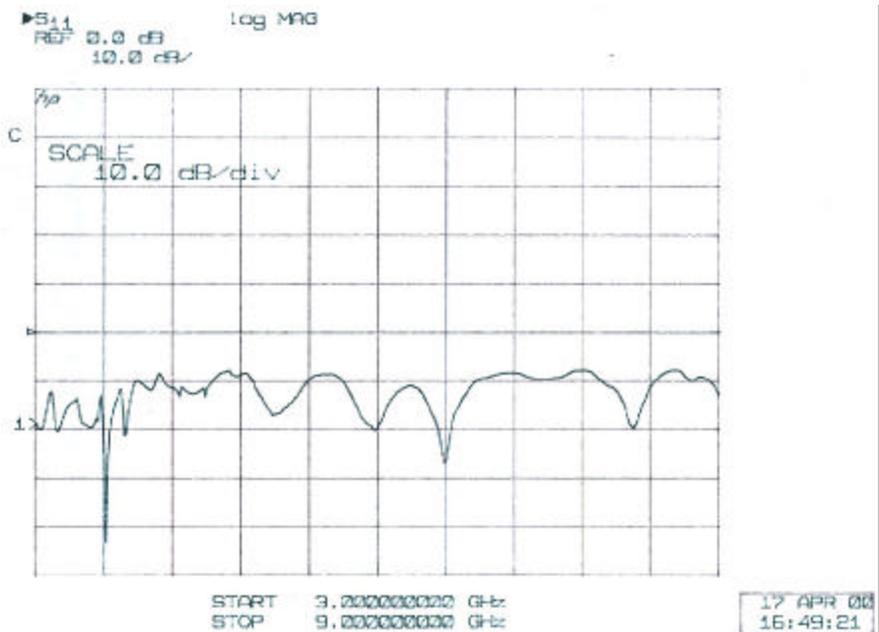


Figure 3: Impedance match through redesigned 4-8 GHz loop.

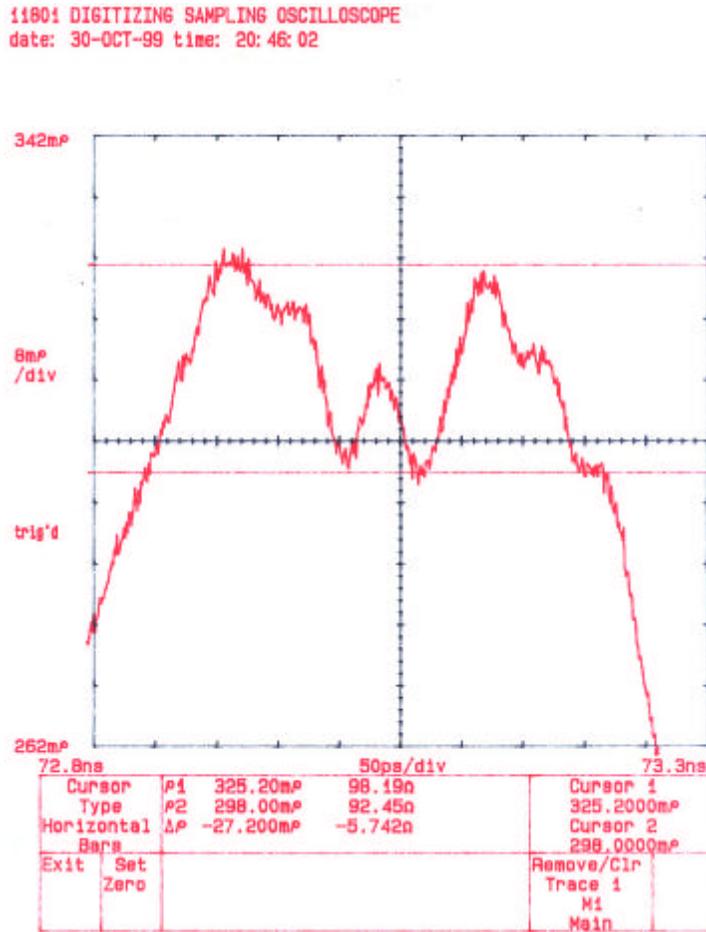


Figure 4: S_{11} of redesigned 4-8 GHz loop.

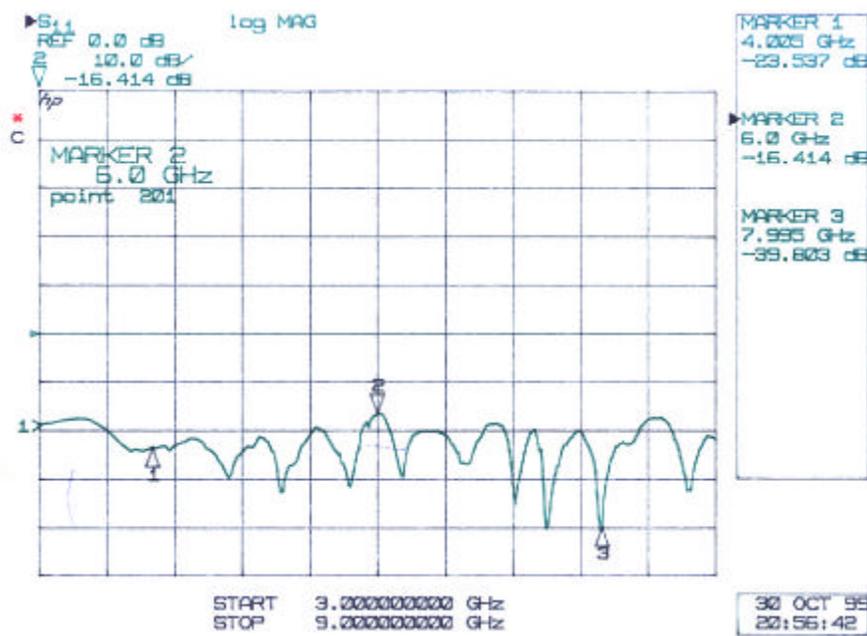


Figure 5: Sensitivity of 4-8 GHz loops.

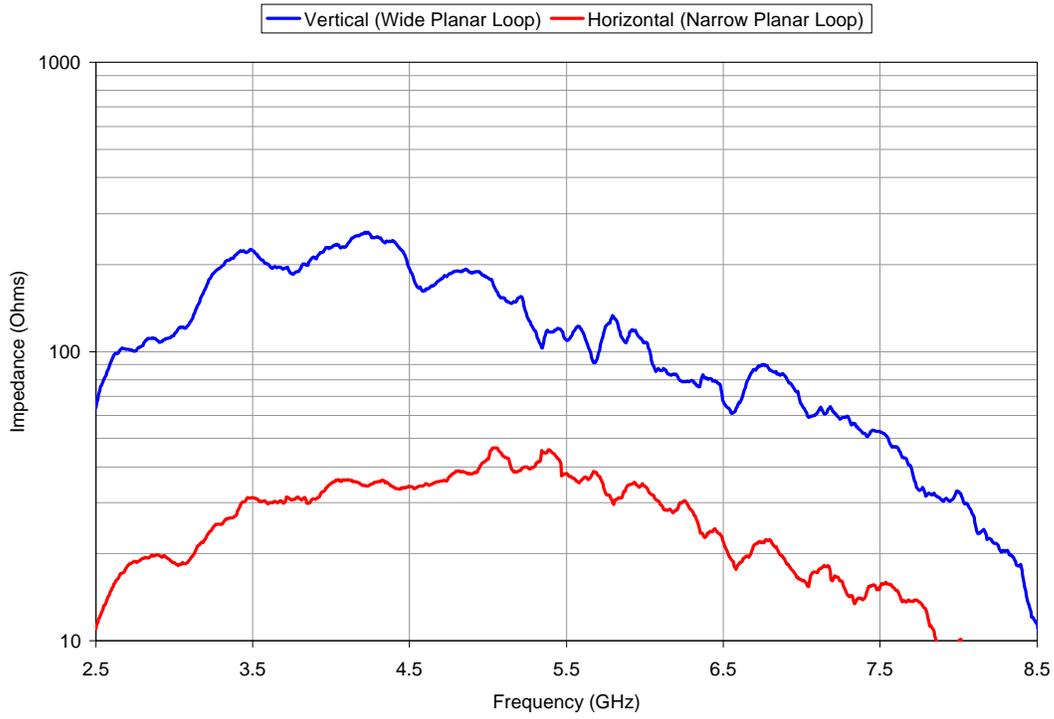


Figure 6: S_{21} through longest and shortest combiner legs.

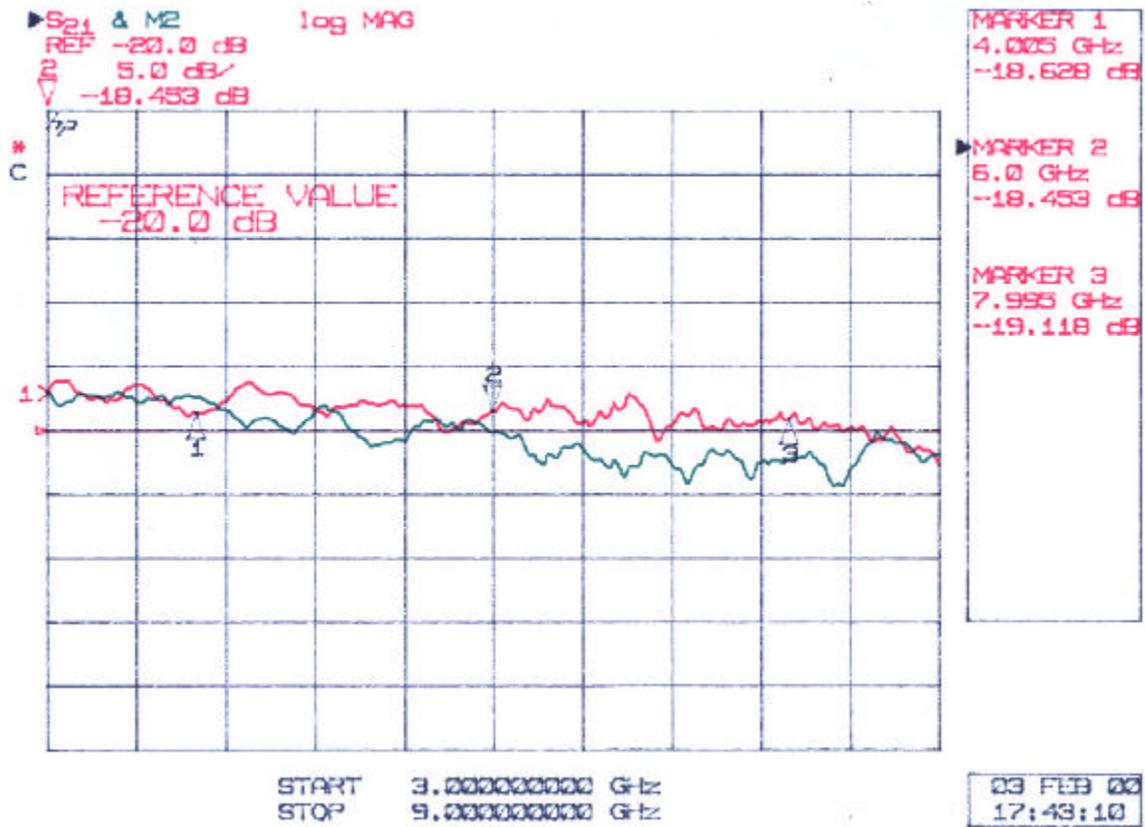


Figure 8: Phase through shortest combiner leg.

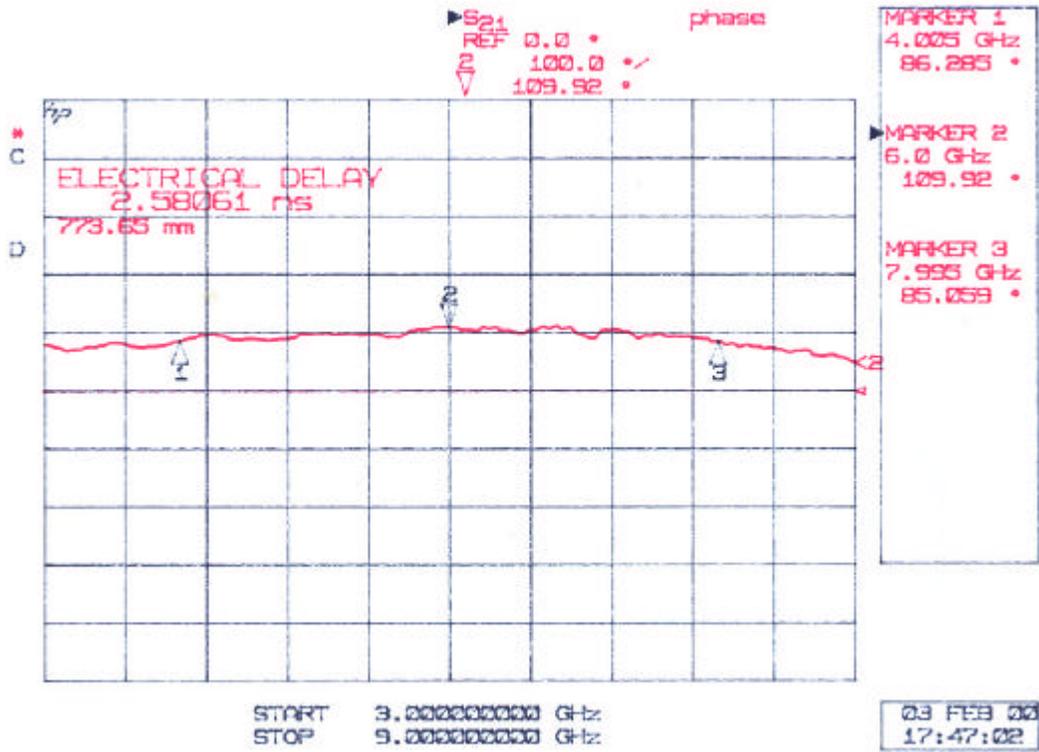


Figure 9: Phase through longest combiner leg.

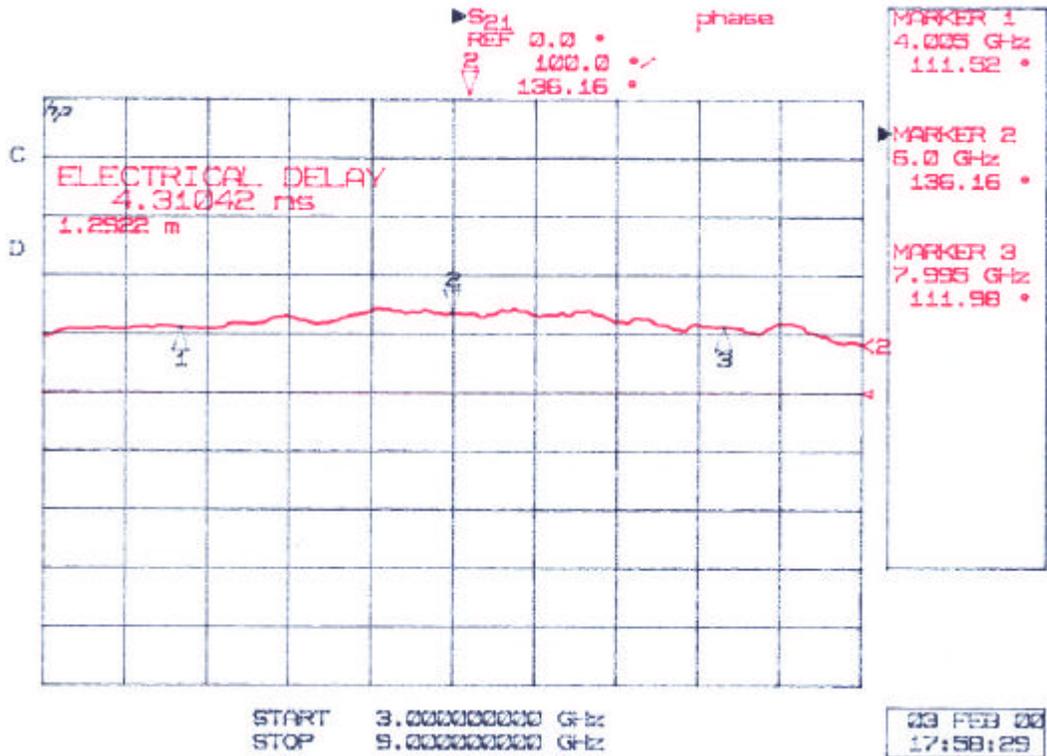


Figure 10: Vector sum of S_{21} data, 4-8 GHz combiner board.

